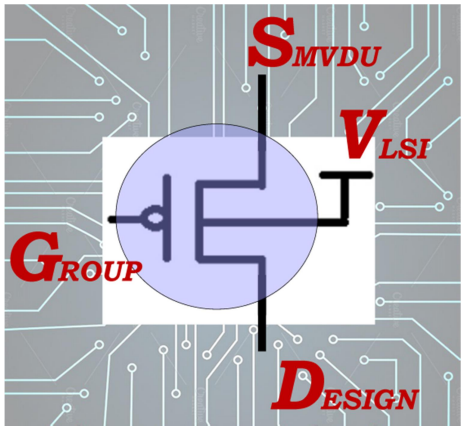
Faculty Development Program

(Under UGC- Malaviya Mission Teacher Training Center – SMVDU)

On

Hands on: Low Voltage and Low PowerAnalog VLSI Design



(29th Jan, 2024 – 02nd Feb, 2024)

School of

Electronics & CommunicationEngineering

Shri Mata Vaishno Devi University

Katra, Jammu & Kashmir-India

About the University

Shri Mata Vaishno Devi University (SMVDU) has been established under the Jammu and Kashmir Shri Mata Vaishno Devi University act, 1999 an Act of the J&K State Legislature as an autonomous, highly Technical & fully Residential University. The University started functioning an academic unit in Aug 2004 when it was inaugurated on 19th August 2004 at the hands of the then Hon'ble President of India Dr. A P J Abdul Kalam. The University is approved by UGC under Section 2(F) & Section 12(B) of UGC Act of 1956

About the Dept. of ECE

The field of electronics is the fastest growing and the most rapidly changing area of technology in the current times. Electronics has become the all-pervasive technology, which finds application in all spheres of engineering including computers, communication, defense, mechatronics, instrumentation, automation, robotics, artificial intelligence, computer networks, satellites, education etc. The use of electronics has brought about a drastic change in the way human civilization exists today. The school is currently focused on providing B.Tech., M.Tech. and Ph.D programs which cover exhaustively the area of Electronics & Communication Engineering.

About the FDP

With the decreasing feature sizes and increasing chip areas, silicon microchips have been broadly doubling their component counts per chip every two years. This relentless exponential growth in the component counts has maintained its trend throughout the eighties also, leaving the VLSI design methods struggling to cope as the actual component counts possible on chips have reached the figure of one million towards the close of the decade. The objective of the FDP is to give an exposure to the participants to the emerging trends and technologies in Low Power Analog VLSI design and device modelling in the scenario of Industry 5.0 revolution. Design techniques that make possible the operation of analog circuits with ultra-low supply voltages, down to 0.5 V will be demonstrated.

Contents

- Issues & challenges in Low voltage & low Power VLSI Design
- Characteristics of scaled MOSFET with reference to down scaling of voltage and power.
- Sub-threshold and super threshold source/drain leakage current models for low- power scaled CMOS design
- Design of Operational Transconductance Amplifiers (OTAs)
- Sub 1- Volt Operational Amplifier Design
- Power Efficient Analog Circuit Design
- Scenario of Analog Design in Industry 5.0

Who Should Attend?

Active researchers, members of academia, scholars and professionals working in the VLSI domain.

Venue

Department of Electronics & Communication Engineering, SMVDU, Katra (J&K)

Important Dates

Last Date of Registration: 19 Jan, 2024

Chief Patron

Prof. (Dr.) Pragati Kumar,
Hon'ble Vice Chancellor, SMVDU

Patron

Sh. Ajay Kumar Sharma (JKAS),
Registrar, SMVDU

Chairman

Dr. Kumud Ranjan Jha
Dean, Faculty of Engg., SMVDU

Organizing Secretary

Dr. Anil Kumar Bhardwaj, Asst. Prof.,
Head, School of ECE, (9419903025)

Coordinators

- **Dr. Vikram Singh, Asst. Prof., SoECE, SMVDU (09466754797)**
- **Dr. Neeraj Tripathi, Asst. Prof., SoECE, SMVDU (09622332957)**

Registration Fee

- **Rs. 3000/- for outside participants (with lodging and boarding)**
- **Rs. 1000/- for outside participants (without lodging and boarding)**
- **No Fee for SMVDU Participants**

The interested participants should register by filling the Google form through the below link: **https://forms.gle/8FYVtQo2MzU1WqD19**

Acc. No.: 0477040100000023
IFSC: JAKA0SMVDUN (5th character is Zero), J&K Bank, SMVDU

Participants need to attach the receipt of the registration fee while filing the registration form.

Certification

Certificate will be issued to the participants after successful submitting the feedback form on completion of the FDP.

Members Organizing Committee

- **Dr. Manish Sabraj**
- **Dr. Sumeet Gupta**
- **Dr. Vijay K. Sharma**
- **Dr. Purnima Hazra**
- **Mr. S. B. Kotwal**
- **Mr. Ashish Suri**

Contact Email

Email: vikram.singh@smvdu.ac.in
neeraj.tripathi@smvdu.ac.in
anil.bhardwaj@smvdu.ac.in

How to Reach SMVDU, Katra (J&K)

The University campus is located 14 km short of the holy town of Katra, and 40 km from Jammu, the campus is well-connected by Road, Rail & Air.