Faculty Profile

Name: Dr. Vijay Kumar Sharma

Designation: Assistant Professor

Department: Electronics & Communication Engineering

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Contact Number and Extn.: 2241

Qualification: B. Tech. (UPTU Lucknow, UP), M. Tech. (NIT Hamirpur, HP), PhD (ABV-IIITM Gwalior, MP)

Experience:

Teaching: 4.0 Years **Research: 6.6 Years**

Areas of Interest / Specialization:

1. Low Power VLSI Design
2. Nanoscale Circuit-Device co-design
3. Low Voltage Electronics
4. Energy Efficient Sub-threshold Logic Operations
5. Variability Aware Circuit Design

Brief Bio-data:

Dr. Vijay Kumar Sharma is Assistant Professor in the Department of Electronics & Communication Engineering since January 2015. He received his *Masters* degree from National Institute of Technology, Hamirpur (HP) in 2009 and *PhD* at ABV – Indian Institute of Information Technology & Management, Gwalior (MP) in 2015. His main research interests are in the areas of VLSI Design. He has published widely in international journals and conferences. He has focused in the last few years on the research issues in process variability in nanoscale regime.

Research Profile

Research Publications:

S. No.	Year	Publication
1	**2010**	Comparison among different CMOS inverters for Low leakage at different Technologies
2	**2010**	Low Power CMOS Inverter design at different Technologies
3	**2011**	Effect of Device Scaling for Low Power Environment
4	**2011**	Study of Leakage Power, Controlled by Input Vector Technique
5	**2013**	Leakage Reduction ONOFIC Approach for Deep Submicron VLSI Circuits Design
6	**2013**	VLSI scaling methods and low power CMOS buffer circuit
7	**2014**	ONOFIC approach: low power high speed nanoscale VLSI circuits design
8	**2014**	PVT variations aware low leakage INDEP approach for nanoscale CMOS circuits
9	**2014**	Techniques for Low Leakage Nanoscale VLSI Circuits: A Comparative Study
10	**2014**	Process, Voltage and Temperature Variations Aware Low Leakage Approach for Nanoscale CMOS Circuits
11	**2014**	High Performance Process Variations Aware Technique for Sub-threshold 8T-SRAM Cell
12	**2015**	INDEP approach for leakage reduction in nanoscale CMOS circuits
13	**2015**	A Reliable Ground Bounce Noise Reduction Technique for Nanoscale CMOS Circuits
14	**2016**	Design of low leakage variability aware ONOFIC CMOS standard cell library
15	**2017**	Design of low leakage PVT variations aware CMOS bootstrapped driver circuit
16	**2017**	An Approach for Low Power Circuit Design using Low Threshold Transistors (Accepted)
17	**2017**	Modified ONOFIC technique for low leakage CMOS circuits (Accepted)

Books/Book Chapter Publications:

S. No.	Year	Publication
1	**2016**	Low-Leakage Techniques for Nanoscale CMOS Circuits

Conference Publications:

S. No.	Year	Conference	Publication
1	2009	National Conference on Recent Trends in Computer & Information Technologies, PIET Panipat, 24-25 Apr. 2009	Leakage reduction techniques: analysis and implementation for nanoscale circuits

2	2016	6th International Conference on Advances in Engineering Sciences and Applied Mathematics (ICAESAM'2016), Kuala Lumpur, Malaysia, 21-22 Dec., 2016	A low leakage input dependent ONOFIC approach for CMOS logic circuits
3	2017	4th International Conference on Signal Processing, Communications and Networking (ICSCN-2017), Madras Institute of Technology, Anna University, Chennai, 16-18 Mar. 2017	Low Leakage Circuit Design using Bootstrap Technique

Award and Honours:

S. No.	Title	Activity/Event	Given by	Year
1	Best paper award	4th IEEE International Conference on Signal Processing, Communications and Networking (ICSCN-2017)	Madras Institute of Technology, Anna University, Chennai	2017
2	GATE 2006	Scholarship	MHRD	2006
3	GATE 2007	Scholarship	MHRD	2007
4	United Scholarship	Scholarship	UP Government	1999
5	Meritorious Scholarship	Scholarship	SIT Mathura (UP)	2003-07
6	Stood 1st Class Position	First Class Position	MIC Pahasu (UP)	2000
7	Stood 1st Class Position	First Class Position	SIT Mathura (UP)	2005

Professional Affiliation:

S. No.	Designation	Organization

1	Reviewer	IEEE Transactions on Very Large Scale Integration (VLSI) Systems
2	Reviewer	IEEE Access
3	Reviewer	International Journal of Electronics
4	Reviewer	Expert Systems With Applications
5	Reviewer	Journal of Circuits, Systems, and Computers
6	Reviewer	IETE Technical Review
7	Reviewer	Electronics Letters
8	Reviewer	Journal of Nanoelectronics and Optoelectronics
9	Reviewer	International Journal of Communication Systems
10	Reviewer	Analog Integrated Circuits and Signal Processing
11	Reviewer	Journal of Computational Electronics
12	Session chair & Technical chair	2nd International Conference on Recent Trends & Advancements in Engineering & Technology
13	Session chair & Technical chair	3rd International Conference on Recent Trends & Advancement in Engineering & Technology, 17-18/11/2016
14	Session chair & Technical chair	4th International Conference on Recent Trends & Advancement in Engineering & Technology, 3-4/11/2017
15	Member of the organizing committee	UGC sponsored Two-day Workshop on “Ultra Low Power Biosensors and Implantable Microsystems”, 2-3/12/2016

16	Member of the organizing committee	UGC sponsored Two-day Workshop on "Numerical Analysis in VLSI CAD using MATLAB and SIMULINK", 14-15/01/2017
17	Coordinator	UGC sponsored One-day Workshop on "Scientific Writing using LaTeX", 24/02/2017

Conference/Workshop/Seminar/Course attended:

1. National Symposium on Nanomaterials Design: Bridging Nanolength scale (NSNMD-2007), 17th Nov. 2007, Advanced Material Science Research Center, NIT Hamirpur (H.P.).
2. Short Term Course on Working & Applications of Electronics Systems (WAES-2008), 4-8th Nov. 2008, Department of Electronics & Communication Engineering, NIT Hamirpur (H.P.).
3. National Conference on Recent Trends in Computer & Information Technologies, 24-25th Apr. 2009, PIET Panipat (H.R.).
4. UGC-HRDC Orientation Programme, 3-30th Jun. 2015, Academic Staff College, Bhagat Phool Singh Mahila Vishwavidyalaya, Sonepat (H.R.).
5. Short Term Course on "Recent Trends in Automobille Engineering", 29 Feb-04 Mar 2016 in collaboration with NITTTR Chandigarh at Shri Mata Vaishno Devi University, Katra (J&K).
6. One day workshop on "Patent drafting and filing", at Shri Mata Vaishno Devi University, Katra (J&K), 20th October, 2016 in Association with TIFAC, Department of Science & Technology, Government of India.
7. One week Short Term Course on "Optimization Using MATLAB", 24-28 Oct 2016 in collaboration with NITTTR Chandigarh at Shri Mata Vaishno Devi University, Katra (J&K).
8. One week workshop on "Cloud Computing", 5-9 Dec 2016 in collaboration with NITTTR Chandigarh at Shri Mata Vaishno Devi University, Katra (J&K).
9. Two week ISTE STTP on CMOS, Mixed Signal and Radio Frequency VLSI Design, (National Mission on Education through ICT), 30/01/2017-04/02/2017, organized by IIT Kharagpur at remote centre Shri Mata Vaishno Devi University, Katra (J&K).
10. 6th International Conference on Advances in Engineering Sciences and Applied Mathematics (ICAESAM'2016), Kuala Lumpur, Malaysia, 21-22 Dec., 2016.
11. 4th IEEE International Conference on Signal Processing, Communications and Networking (ICSCN-2017), Madras Institute of Technology, Anna University, Chennai, 16-18 Mar. 2017.
12. UGC HRDC Refresher Course 10th -30th May 2017 at HRDC Punjabi University, Patiala (PB).