



Shri Mata Vaishno Devi University

Kakryal, Katra- 182320 (J&K)

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School of Electronics & Communication Engineering

Time Table (Major Examinations)

Semester 1 - M.Tech E&CE

November - Odd Semester - 2018-19

Date / Day	Time	Subject / Title	Room No.	Student Entry No.	Invigilator
25/11/2018 Sunday	09:30 AM - 12:30 PM	Advanced Digital Communications (ECL 6150)	Hall - D 107	,18MMC001-18MMC018	Dr. Rakesh Kumar Jha
26/11/2018 Monday	09:30 AM - 12:30 PM	Signal Processing Techniques and Applications (ECL 6182)	Hall - D 107	,18MMC001-18MMC018	Mr. Ashish Suri
28/11/2018 Wednesday	09:30 AM - 12:30 PM	Wireless Networks and Protocols (ECL 6110)	Hall - D 107	,18MMC001-18MMC018	Dr. Sachin Kumar Gupta
30/11/2018 Friday	02:00 PM - 05:00 PM	Research Methodologies (BUL 8223)	Hall - D 107	,18MMC001-18MMC018	Dr. Sandeep Bhogal
1/12/2018 Saturday	09:30 AM - 12:30 PM	Integrated Circuit Design (ECL 6221)	Hall - D 107	,18MMC001-18MMC018	Dr. Vijay Kumar Sharma



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Time Table (Major Examinations)

Semester 3 - M.Tech E&CE

November - Odd Semester - 2018-19

Date / Day	Time	Subject / Title	Room No.	Student Entry No.	Invigilator	Time	Subject / Title	Room No.	Student Entry No.	Invigilator
22/11/2018 Thursday	09:30 AM - 12:30 PM	Embedded System Design (ECL 7084)	Hall - C 111	,17MMC001-17MMC018	Mr. Swastik Gupta					
25/11/2018 Sunday	09:30 AM - 12:30 PM	Internet of Things (IOT) (ECE 6111)	Hall - C 111	,17MMC001-17MMC018	Dr. Rakesh Kumar Jha	09:30 AM - 12:30 PM	Advanced CMOS VLSI Design (ECE 6230)	Hall - C 111	,17MMC001- 17MMC018	Mr. Anil Kumar Bhardwaj
28/11/2018 Wednesday	02:00 PM - 05:00 PM	Economics of Natural Resources (SEL 2062)	Hall - LT 2 LT 4	, 17MMC010, 17MMC003, 17MMC004, 17MMC001, 17MMC017, 17MMC013, 17MMC002, 17MMC009, 17MMC006, 17MMC007, 17MMC018, 17MMC014, 17MMC016, 17MMC012, 17MMC008, 17MMC005, 17MMC015, 17MMC011	Mr. Anil Kumar Bhardwaj					