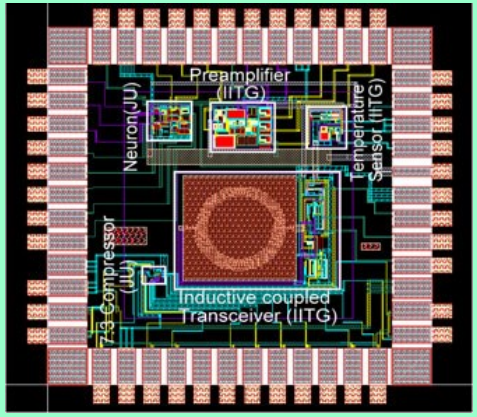
Faculty Development Program

on

"VLSI Design and Fabrication in the Scenario of Industry 5.0"



20th March 2023 to 24th March 2023

Organized By:-

School of Electronics & Comm. Engg.,

Shri Mata Vaishno Devi University,

Katra, J&K, 182320. www.smvdu.ac.in

About the University

Shri Mata Vaishno Devi University (SMVDU) has been established under the Jammu and Kashmir Shri Mata Vaishno Devi University act, 1999 an Act of the J&K State Legislature as an autonomous, highly Technical & fully Residential University. The University started functioning an academic unit in Aug 2004 when it was inaugurated on 19th August 2004 at the hands of the then Hon'ble President of India Dr. A P J Abdul Kalam. The University is approved by UGC under Section 2(F) & Section 12(B) of UGC Act of 1956

About the School of Electronics & Communication Engineering, SMVDU

The field of electronics is the fastest growing and the most rapidly changing area of technology in the current times. Electronics has become the all-pervasive technology, which finds application in all spheres of engineering including computers, communication, defense, mechatronics, instrumentation, automation, robotics, artificial intelligence, computer networks, satellites, education etc. The use of electronics has brought about a drastic change in the way human civilization exists today. The school is currently focused on providing B.Tech., M.Tech. and Ph.D programs which cover exhaustively the area of Electronics & Communication Engineering.

About the FDP

With the decreasing feature sizes and increasing chip areas, silicon microchips have been broadly doubling their component counts per chip every two years. This relentless exponential growth in the component counts has maintained its trend throughout the eighties also, leaving the VLSI design methods struggling to cope as the actual component counts possible on chips have reached the figure of one million towards the close of the decade. The objective of the FDP is to give an exposure to the participants to the emerging trends and technologies in VLSI design and device modelling in the scenario of Industry 5.0 revolution.

Target Participants

Faculty from University and Colleges, Research Scholars, and Industry persons.

Mode of lecture: Offline & Online.

Mode of Joining FDP:
Online / Offline (for Outside Participants)
Offline Only (for Internal Participants)

Registration Information

Fee: Rs. 1000 (for External Participant)

A/c No.: 0477040100000023 J&K Bank, SMVDU

IFSC Code JAKA0SMVDUN (middle is zero & there is no space)

How to Apply: Applicants should apply through Google Form. Last date of application: **19.03.2023**

Google Form Link for Registration:
https://docs.google.com/forms/d/e/1FAIpQLSeIKnmXWeruu5PtAo_WSMV_T_5YyRqCZsBRahca6KI9GPdvEA/viewform?usp=sf_link

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