श्री माता वैष्णो देवी विश्वविद्यालय
Shri Mata Vaishno Devi University
Kakryal, Katra – 182 320 (J&K)

SMVDU/R&D/2021/4527-4752 Date: 31.08.2021

NOTIFICATION

Sub: List of Candidates Provisionally Shortlisted for Admission to Ph.D. Program in Electronics & Communication Engineering offered by School of Electronics and Communication Engineering, at SMVDU – Phase I

The following candidates have been provisionally short listed by the SRC of SoECE for admission to Ph.D. program in Electronics and Communication Engineering, offered by School of Electronics and Communication Engineering, SMVDU for the Academic Session 2021 -22:

Sl.	Name	Parentage	Admit No.	Eligible
1.	SAILA	ALTAF HUSSAIN	ECE101	Eligible for written test
2.	SHATRUGHAN	SH JAGAN NATH	ECE102	Eligible(Gate), no entrance exam
3.	ANKIT	RAJENDER SINGH	ECE103	Eligible for written test
4.	EKTA JOLLY	ROUNAQ LAL JOLLY	ECE104	Eligible(Gate), no entrance exam
5.	NAYARAH SHABIR KHAN	SARDAR SHABIR AHMED KHAN	ECE105	Eligible for written test
6.	SATISH	RAM NIWAS	ECE106	Eligible for written test

The Provisionally Shortlisted candidates who are NET / GATE / SLET /M .Phil. qualified are exempted from appearing in Ph.D. admission written test and will directly appear in the presentation/ interview in person on 10th September 2021 and candidates who are non -GATE/NET/ SLET/M. Phil. qualified, shall have to appear in written test as well as interview, to be conducted on 10th September 2021. The candidates are hereby informed that they must report for written test and/or interview / presentation to the School of Electronics and Communication Engineering, as per the schedule mentioned below:

Sl.	Particulars	Expected Timing
1	Reporting Time for Non UGC/CSIR/AICTE - NET / GATE/SLET / M .Phil. qualified candidates	Forenoon session on 10.09.2021 (timing to be intimated by the school)
2	Document Verification for Non UGC/CSIR/AICTE - NET/ GATE / SLET/ M .Phi l. qualified candidates	
3	Entrance Test for Non UGC/CSIR/ AICTE - NET/ GATE / SLET/ M.Phil. qualified candidates	
4	Reporting Time for UGC/CSIR/ AICTE - NET / GATE / SLET/ M.Phil. qualified candidates for interview	Forenoon session on 10.09.2021 (timing to be intimated by the school)
	Document Verification for UGC/CSIR/ AICTE - NET / GATE / SLET/ M.Phil. qualified candidates	
5	Presentation / Interview for UGC/CSIR/AICTE - NET / GATE / SLET/ M .Phil. qualified candidates	
6	Presentation / Interview for Non UGC/ CSIR/AICTE- NET/ GATE / SLET / M.Phil. candidates who have qualified the entrance test	Afternoon session on 10.09.2021 (timing to be intimated by the school)

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Important points

1. The result of the Written Test will be displayed on the University website www.smvdu.ac.in and the School Notice Board on 10.09.2021 in the afternoon by the Chairman, SRC of SoECE.
2. The Entrance written test shall consist of Multiple Choice Objective Type Questions [MCQs) of the level of Post Graduate Degree examination in Physics [50% subject related and 50% Research Methodology]
3. UGC/CSIR/ AICTE - NE T / GATE/ SLET/M.Phil. qualified candidates who are exempted from appearing in Ph.D. admission written test will directly appear in the presentation / interview.
4. All provisionally shortlisted candidates must come prepared with a 10 minutes presentation (MS PPT).
5. All primarily shortlisted candidates are required to bring all original documents and their self-attested photocopies (high school, intermediate , graduation, post-graduation, NET/SLET/GATE/M.Phil. etc.), in support of their claim as mentioned in the Ph.D. Application Form. They must carry a valid photo identification card like Adhaar / passport / government Id card / PAN card, etc.
6. Candidates in Government / Private / University services are required to submit the No Objection Certificate from their employer.
7. All provisionally shortlisted candidates must submit documentary proof in respect of their claim to their eligibility on the date of written test and interview, or else they shall not be allowed to appear in the written test and interview.
8. The Head of the concerned shall submit the final result along with application forms and related documents through SRC of the School and Dean of the Faculty concerned to R&D Section for seeking approval of the Competent Authority.
9. For any queries, Head of the School can be contacted on 01991-285524 Extn: 2326 or email id hod.dece@smvdu.ac.in

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Registrar

Note: No claim for TD/DA shall be entertained.

Copy to
1. Dean FoE for Information
2. Dean [R&D] for Information
3. Head School of Electronics and Communication Engineering for information and compliance.
4. PS to VC for kind information of the Hon'ble Vice Chancellor.
5. I/c Website, for uploading the same on the University Website.
6. Concerned File